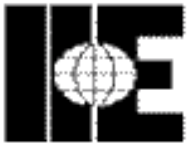


1st Annual IIE/Tefen Graduate Student Competition: Excellence in Industrial Engineering

Case Study

Ultra Silicon Devices, Inc.

Version 1.0

November 1998

1- Abstract

Semiconductor chips are fabricated by "printing" integrated circuits (ICs) onto silicon wafers—ICs are made by creating and interconnecting many thousands of transistors on a very small piece of silicon. The first step in the fabrication process is the actual design of the IC (or "layout design"). Once this layout is tested for accuracy and functionality, a mask (or reticle) is generated to be used in the photolithography process. It is at this critical process where the different layers of the IC are "projected" onto the silicon wafer.

USD, Inc. (Ultra Silicon Devices, Inc.) is a designer and fabricator of chips with $1.7 Billion revenues in 1997. The Design Reliability Group (DRG), within USD, is in charge of inspecting all "layout designs" before they are released to the mask manufacturer. These designs are sent to DRG by a number of "design houses" around the world. The inspection process involves testing the reliability of the designs through the use of state-of-the-art CAD/CAM software running on high-end workstations. If errors are found, the design could be reworked internally by DRG (if they are simple fixes) or sent back to the design house for corrective action. DRG's environment is characterized by its poor forecasting visibility, the high variability in test run times, the highly unpredictable corrective action cycles, and the breadth of design technologies (at different life cycles) used by USD. In this volatile environment, DRG's current capacity planning capabilities are seriously limited.

Thus, your team is hired to design in 4 months a planning system that will most accurately predict DRG's resource requirements (technicians, engineers, software licenses, and workstations) in order to reduce cycle times and improve on time delivery.

2 - Work Flow

In the past, DRG has performed design testing in a linear format (see Exhibit 1). When the design package arrives from the client it is checked to ensure that all relevant and necessary information is included. If there is anything missing from the required files and information, the package is returned to the design house with a notification of which necessary materials are missing. The first test has been the Physical Connection Test (PCT). At this stage, the design is analyzed to discover if any connections are broken or missing. The second test is the Logical Evaluation Test (LET). Here the design is

scrutinized for mistakes in the logical operations. Each of these tests is made on large mainframe computers running licensed software. Currently there are 4 licenses for the physical examination, 8 for the logical test and a total of 10 mainframes. After testing completion, the design proceeds to the Mask Format where the final design is compiled and physically prepared for release.

3 - Testing Procedures

In the linear testing order, a given design was always required to pass through the Physical Connection Test (PCT) before being sent on to the Logical Evaluation Test (LET). If the design fails the LET after passing the PCT, the new design created by correcting the logical defects must again pass through the PCT before being reevaluated at the LET. In theory, the two operations can be performed in parallel so that a design can be tested for both types of defects concurrently and pass directly to Mask Format upon release (see Exhibit 2). The only constraint on the system is that the design released to Mask Format must have passed through each test in its current revision. The reasoning behind the current linear process is that there will almost always be logical defects in a circuit design in which there are physical incongruities. So, by fixing the physical connections first, many problems which would cause a flag to be raised during the LET would be fixed without the time and trouble of testing. The manager of the DRG has informed you that historically if a design failed the LET after passing the PCT, the corrected design has a 7% probability of failing the PCT upon retest. The technician is not required to be at the testing station while the program is running. The PCT and LET software perform all analysis without the assistance of a technician. However, the technician is required to load and unload the design onto the mainframe for analysis. The programs do not perform the analysis at constant rates (the program is stochastic in nature although the variable(s) which controls the run length is(are) not known to DRG) and the run times can vary greatly (see Exhibit 3). The main factors which are believed to affect the run time are design complexity, number of transistors, and the # of design errors. The problem is that if the program finds a fundamental flaw in the initial analysis, it will continue to run to completion, wasting valuable workstation and license time. Errors are just as likely to appear on the screen at any time during the testing period.

The testing facility works around the clock when necessary, sometimes staffed at all hours. DRG feels that to properly monitor each testing mainframe, one technician is required for every four to five operating mainframes. Furthermore, one engineer should be on hand to oversee the operations of every three technicians. Currently, workers are on line for shifts of 12 hours for 3 or 4 days (alternating) a week.

4 - Workforce

As noted above, there are two levels of expertise within DRG: technicians and engineers. The technicians are primarily in charge of receiving the data, loading and unloading the designs for testing, packaging the analyzed design during mask format and returning it to the design house. Technicians also perform maintenance on the equipment within the facility. The engineers make the decision on whether to attempt to fix the design problem in-house or return to the designer for rework. The engineers are also in charge of error correction, training, internal experiments and machinery failure.

5 - Database

DRG utilizes a Traveler to track the cycle time of each order. The data provided by DRG in Tables 1-4 is taken directly from these Travelers. When an order arrives, the cycle time begins and the date received is recorded. After each stage in the process the first successful test completion date is recorded. Whenever a design fails a given test it is either fixed by the USD engineer on hand or returned to the design house for rework (historically, USD engineers have been able to fix 94% of all physical connection errors and 72% of all logical design failures). In either case, the date of the failed test completion is not recorded. After being edited, the new design is retested and if it passes the test, the successful run completion date will be recorded. Thus, *the data in the table is the date which the design first completed the given test successfully*. In the case where the design is returned to the PCT after failing the LET analysis, the date the design successfully passes the PCT the second time is *not* recorded. All values provided show the first-pass date. The final two columns in Table 1 show the number of times that each device failed the two primary tests. DRG recognizes that this is probably not the optimal way to collect data but this is the available process currently.

6 - Clients

DRG performs design inspection for a variety of clients. The first, and most common design group is USD, the company which operates DRG. Because of DRG's special expertise in the area of design analysis and certification, international integrated circuit manufacturers worldwide send their designs to DRG for analysis. Firms from Europe, Japan, USA and Canada all utilize the service DRG provides. Tables 1-4 give the country source for each design ID tested over the past 4 months. DRG suspects that the number of errors and the cycle time of a given design are not only dependent on technology and the number transistors but also on the source of the design.

7 - Technologies and the Competitive Market

As indicated above, forecasting is one of the most difficult problems that DRG is facing and much of the complication comes from the nature of the Integrated Circuit industry with its high turnover in product technology. For any company to stay competitive with its peers, it must be continually developing newer technology and upgrading products at a constant rate. This makes estimating the required number of mainframes and licenses difficult to estimate. For example, DRG performed analysis for 23 instances of technology GRA6000 during the past four months but only expects 2 more instances during months 9-12. The information on testing time found in Exhibit 3 is only for the past four months with the particular product mix which those months covered.

8 - Forecasting

The final exhibit provided is DRG's forecast for months 9-12 of operations (Exhibit 4). Although the information is not 100% reliable, the estimates given to DRG by its clients are usually a close approximation of reality. There is concern that as the demand grows, the current number of licenses and mainframes will not be sufficient to test the required number of designs. DRG can requisition more mainframes from other areas of operation within USD if they are required but there is generally a one month lead time in receiving the requested stations. New licenses arrive immediately upon order because the only thing required is a new registration number from DRG's vendor. As for staffing constraints, 2-3 months are required to hire and train a technician while engineers can be hired with 1-month notice.

9 - The Project

DRG has provided your team with actual data for the first four months of the year regarding the product mix and cycle times, processing time analysis, and a forecast of the expected demand by technology and country for months 9-12 of this year. It is now the start of month five and you have been given 4 months with which to provide DRG with a modeling system including:

- Quantitative Analysis
- Resource Modeling
- Methodology to use and maintain the proposed system

Exhibit 1: DRG Linear Process Flow (Current)

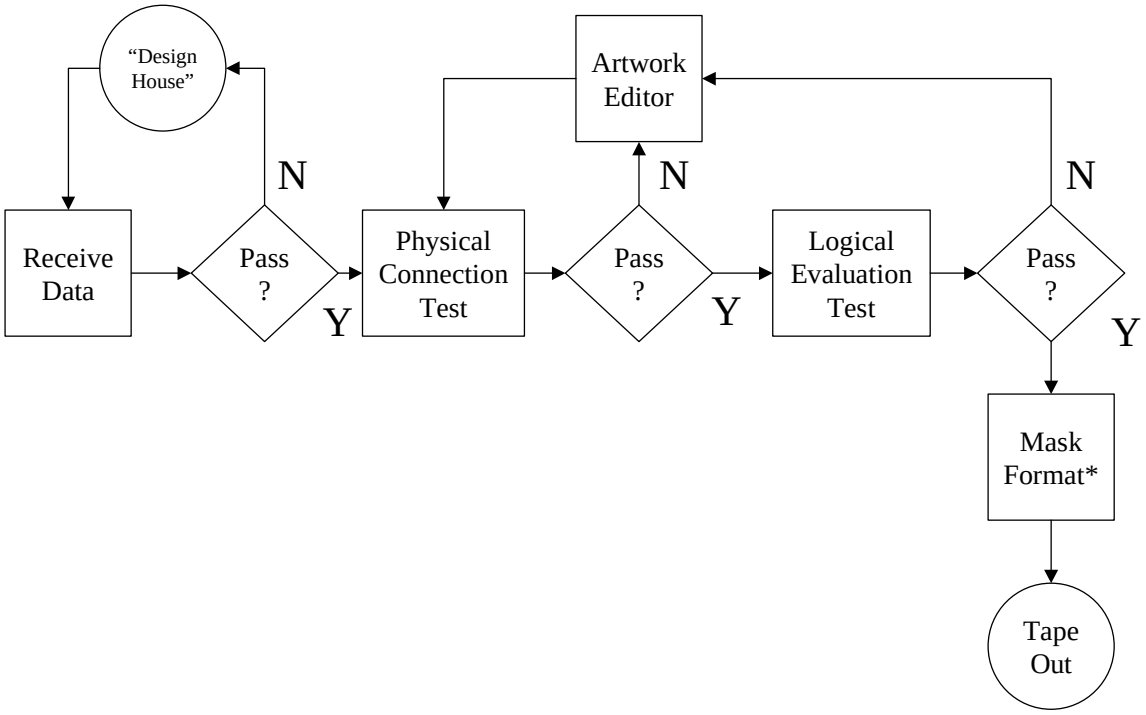
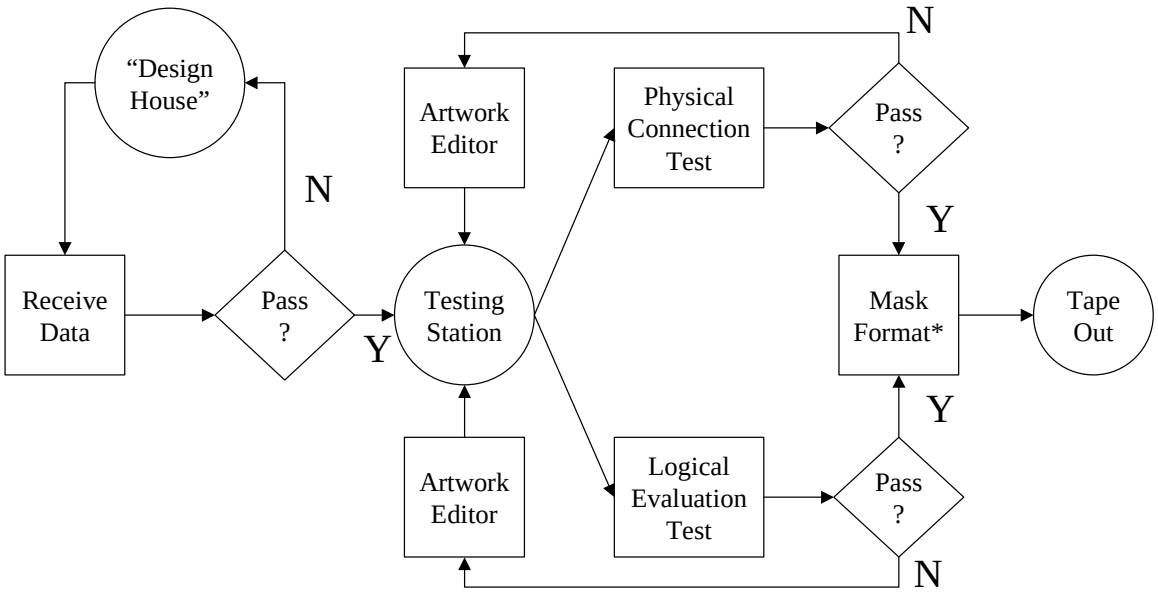


Exhibit 2: DRG Parallel Process Flow



*Before Mask Format can be performed, the same design must pass both the Physical and the Logical Tests.

Table 1: Month 1 Traveler Data

Technology	Device ID#	Country	# of Transistors	Receive Date	Data Check	Physical Test	Logical Test	Mask Format	Incidents of Physical Failure	Incidents of Logical Failure
GRA6000	aa09283	USD	46,125	1/2	1/3	1/5	1/5	1/6	1	0
	aa09828	USD	103,763	1/8	1/8	1/11	1/11	1/17	1	0
	aa39200	USD	108,644	1/10	1/11	1/11	1/13	1/15	0	1
	aa39502	USD	56,887	1/11	1/13	1/14	1/15	1/19	2	0
	aa49502	USD	98,327	1/19	1/19	1/20	1/22	1/24	1	1
	bb92823	USA	35,222	1/2	1/2	1/3	1/8	1/9	0	3
	bb02394	USA	48,655	1/4	1/4	1/5	1/7	1/11	0	1
	bb29304	USA	10,578	1/5	1/6	1/7	1/9	1/20	1	1
	bb03923	USA	88,631	1/8	1/8	1/10	1/11	1/13	1	0
	bb93283	USA	54,876	1/16	1/18	1/18	1/19	1/21	2	1
	ff29283	Asia	123,267	1/6	1/6	1/9	1/9	1/10	2	0
	T00014	Test	66,883	1/26	1/26	1/27	1/28	1/30	1	1
Avg.	**12**		**70,155**						**1.00**	**0.75**
		Sum	841,858							
GRA7000	aa75829	USD	1,799,969	12/30	1/6	1/6	1/8	1/12	0	2
	aa94022	USD	318,182	1/4	1/8	1/9	1/10	1/10	1	1
	aa39204	USD	610,658	1/7	1/11	1/13	1/14	1/15	1	0
	aa49382	USD	1,919,985	1/22	1/25	1/25	1/25	1/26	0	0

	cc94293	Canada	2,151,124	1/18	1/22	1/22	1/23	1/25	0	1
	cc29304	Canada	872,460	1/22	1/24	1/25	1/27	1/27	1	2
	ee92029	Japan	333,570	1/6	1/13	1/15	1/17	1/18	1	1
	ee84922	Japan	246,817	1/17	1/18	1/18	1/19	1/21	0	1
	ff19384	Asia	1,860,311	1/1	1/5	1/6	1/7	1/9	1	2
	T92384	Test	1,351,894	1/24	1/26	1/26	1/28	1/28	1	2
Avg.	**10**		**1,146,497**						**0.60**	**1.20**
		Sum	11,464,970							
GRA8500	aa67858	USD	137,902	12/24	12/25	12/28	1/3	1/5	2	4
	bb23948	USA	1,439,815	12/29	12/30	1/1	1/4	1/6	0	2
	cc39109	Canada	581,131	1/13	1/15	1/17	1/21	1/23	1	2
	cc33244	Canada	1,156,884	1/5	1/5	1/6	1/8	1/10	1	1
	cc23125	Canada	1,567,884	1/8	1/8	1/9	1/10	1/12	1	1
	cc93239	Canada	840,689	1/11	1/12	1/12	1/15	1/18	0	1
	cc48593	Canada	354,719	1/15	1/16	1/17	1/20	1/21	0	2
	cc02034	Canada	1,893,544	1/17	1/18	1/21	1/26	1/27	2	4
	cc02139	Canada	2,808,991	1/20	1/20	1/21	1/22	1/22	1	0
	cc99230	Canada	750,986	1/22	1/25	1/25	1/26	1/28	0	0
	cc67903	Canada	356,489	1/22	1/22	1/24	1/24	1/27	1	0
	cc09220	Canada	1,435,228	1/23	1/24	1/25	1/28	1/30	1	2
	dd92338	Europe	1,496,656	1/2	1/3	1/5	1/8	1/17	1	2
	ee99229	Japan	860,721	1/6	1/6	1/7	1/9	1/10	0	1
	ee78829	Japan	2,181,721	1/20	1/20	1/26	1/27	1/30	4	0
Avg.	**15**		**1,190,891**						**1.00**	**1.47**
		Sum	17,863,360							
GZN0100	aa39409	USD	1,856,124	12/30	1/1	1/8	1/10	1/16	4	1
	aa00392	USD	1,156,495	1/5	1/6	1/9	1/10	1/14	1	1
	aa39404	USD	540,658	1/11	1/13	1/13	1/15	1/16	0	2
	aa59402	USD	782,356	1/11	1/14	1/15	1/17	1/19	1	1

	aa92042	USD	115,684	1/17	1/20	1/22	1/24	1/29	1	3
	bb47893	USA	2,568,189	1/8	1/10	1/10	1/12	1/13	0	3
	2									
	bb93004	USA	1,783,246	1/12	1/13	1/13	1/17	1/20	1	5
Avg.	**7**		**1,257,536**						**1.14**	**2.29**
		Sum	8,802,752							
GZN2000	bb89293	USA	345,668	1/5	1/5	1/6	1/8	1/12	1	2
	bb00930	USA	1,558,871	1/8	1/9	1/11	1/12	1/15	1	1
	bb38392	USA	965,884	1/9	1/9	1/11	1/15	1/16	2	3
	bb20388	USA	1,168,972	1/11	1/11	1/16	1/17	1/19	4	0
	bb09332	USA	1,759,663	1/20	1/20	1/21	1/22	1/23	0	2
Avg.	**5**		**1,159,812**						**1.60**	**1.60**
		Sum	5,799,058							
XTL0001	T85623	Test	1,259,987	1/2	1/2	1/3	1/5	1/9	1	3
	T78925	Test	2,677,943	1/5	1/5	1/11	1/15	1/21	9	5
	T23495	Test	1,658,324	1/5	1/6	1/8	1/12	1/15	2	3
Avg.	**3**		**1,865,418**						**4.00**	**3.67**
		Sum	5,596,254							

Table 2: Month 2 Traveler Data

Technology	Device ID#	Country	# of Transistors	Receive Date	Data Check	Physical Test	Logical Test	Mask Format	Incidents of Physical Failure	Incidents of Logical Failure
GRA6000	aa55789	USD	105,657	1/30	1/30	2/1	2/3	2/6	1	2
	aa24489	USD	68,544	2/1	2/1	2/3	2/5	2/6	2	1
	aa45224	USD	216,846	2/6	2/7	2/9	2/10	2/12	1	2
	aa13257	USD	100,685	2/12	2/13	2/14	2/14	2/16	1	0
	aa19755	USD	86,648	2/18	2/18	2/20	2/22	2/25	3	1
	aa21895	USD	54,933	2/21	2/21	2/22	2/25	2/26	0	3
	bb54775	USA	78,561	2/4	2/4	2/7	2/10	2/11	4	2
	bb24978	USA	102,688	2/18	2/19	2/20	2/21	2/23	1	1
Avg.	**8**		**101,820**						**1.63**	**1.50**
		Sum	814,562							
GRA7000	aa84623	USD	400,856	2/1	2/1	2/3	2/6	2/8	2	2
	aa12844	USD	2,544,686	2/8	2/9	2/10	2/14	2/15	0	3
	aa69856	USD	1,266,584	2/10	2/12	2/14	2/15	2/17	1	1
	bb88465	USA	458,622	2/18	2/18	2/19	2/22	2/23	1	2
	cc87662	Canada	987,221	1/25	1/28	2/1	2/3	2/3	4	2
	cc79521	Canada	1,789,925	2/3	2/4	2/5	2/6	2/8	1	0
	cc19886	Canada	750,998	2/5	2/5	2/7	2/10	2/11	1	2

	ff78997	Asia	1,325,449	2/14	2/14	2/17	2/20	2/22	2	1
Avg.	**8**		**1,190,543**						**1.50**	**1.63**
		Sum	9,524,341							
GRA8500	aa48991	USD	225,668	2/5	2/5	2/7	2/15	2/16	2	6
	aa28488	USD	1,566,844	2/20	2/21	2/22	2/25	2/26	1	2
	bb68877	USA	265,433	2/3	2/3	2/3	2/7	2/10	0	4
	bb87995	USA	1,266,584	2/7	2/7	2/10	2/11	2/12	2	1
	bb12557	USA	2,166,844	2/11	2/12	2/16	2/17	2/17	3	0
	cc78992	Canada	766,522	1/27	2/1	2/2	2/4	2/4	1	0
	cc24668	Canada	866,211	2/1	2/1	2/6	2/7	2/7	2	1
	cc24997	Canada	1,756,889	2/2	2/2	2/5	2/7	2/9	3	1
	cc57994	Canada	2,154,998	2/4	2/6	2/9	2/10	2/11	2	2
	cc79221	Canada	850,446	2/8	2/8	2/12	2/14	2/14	5	1
	cc96785	Canada	433,255	2/15	2/16	2/17	2/24	2/24	0	5
	cc78991	Canada	1,896,622	2/16	2/16	2/19	2/22	2/23	0	2
	dd57798	Europe	1,266,854	2/7	2/8	2/13	2/15	2/16	5	1
	dd78997	Europe	750,668	2/8	2/9	2/14	2/15	2/16	4	2
	dd21665	Europe	1,204,998	2/11	2/12	2/16	2/19	2/21	2	1
	ee62216	Japan	1,899,522	2/13	2/13	2/15	2/17	2/19	2	2
	ee21668	Japan	652,115	2/4	2/4	2/5	2/7	2/7	0	2
Avg.	**17**		**1,175,910**						**2.00**	**1.94**
		Sum	19,990,473							
GZN0100	aa54889	USD	520,665	1/31	2/1	2/5	2/9	2/11	3	1
	aa25466	USD	789,665	2/2	2/2	2/8	2/11	2/13	5	2
	aa52166	USD	2,156,655	2/2	2/3	2/6	2/9	2/10	4	3
	aa26799	USD	1,523,882	2/4	2/5	2/7	2/10	2/11	0	3
	aa98755	USD	897,553	2/16	2/16	2/21	2/24	2/25	3	2
	aa52168	USD	1,102,665	2/18	2/18	2/22	2/27	2/27	2	4
	bb78995	USA	650,899	2/1	2/1	2/3	2/8	2/10	1	3

	bb79882	USA	1,216,887	2/12	2/12	2/19	2/21	2/21	8	1
	bb35546	USA	1,452,668	2/12	2/13	2/16	2/19	2/20	2	2
Avg.	**9**		**1,145,727**						**3.11**	**2.33**
		Sum	10,311,539							
GZN2000	bb78995	USA	897,882	2/9	2/9	2/15	2/18	2/19	6	2
	bb45228	USA	1,456,332	2/11	2/11	2/16	2/18	2/18	4	1
	bb79252	USA	856,211	2/12	2/12	2/21	2/24	2/26	9	2
	bb46897	USA	1,423,494	2/18	2/19	2/22	2/25	2/25	2	1
	T78921	Test	2,001,658	2/1	2/1	2/4	2/7	2/8	1	0
	T00198	Test	1,898,246	2/1	2/2	2/6	2/10	2/11	3	3
Avg.	**6**		**1,422,304**						**4.17**	**1.50**
		Sum	8,533,823							
XTL0001	aa26685	USD	2,568,499	2/3	2/4	2/9	2/14	2/15	4	3
	T52668	Test	1,654,249	2/6	2/8	2/12	2/13	2/14	5	0
	T79553	Test	1,892,544	2/12	2/12	2/15	2/21	2/22	2	7
Avg.	**3**		**2,038,431**						**3.67**	**3.33**
		Sum	6,115,292							

Table 3: Month 3 Traveler Data

Technology	Device ID#	Country	# of Transistors	Receive Date	Data Check	Physical Test	Logical Test	Mask Format	Incidents of Physical Failure	Incidents of Logical Failure
GRA6000	aa49502	USD	113,548	3/1	3/1	3/4	3/7	3/7	3	2
	aa29034	USD	70,563	3/11	3/12	3/13	3/14	3/16	0	1
	bb05321	USA	98,521	3/9	3/10	3/10	3/11	3/12	0	1
Avg.	**3**		**94,211**						**1.00**	**1.33**
		Sum	282,632							
GRA7000	aa24955	USD	500,789	3/3	3/3	3/7	3/8	3/12	3	0
	aa78620	USD	1,478,955	3/8	3/9	3/11	3/12	3/13	2	1
	bb78952	USA	1,756,324	3/1	3/1	3/4	3/6	3/6	2	1
	bb74261	USA	745,065	3/21	3/22	3/23	3/27	3/29	0	3
	cc78952	Canada	1,352,789	3/3	3/4	3/6	3/9	3/11	2	3

	cc79523	Canada	624,532	3/5	3/5	3/8	3/10	3/10	4	2
	ff78785	Asia	1,856,234	3/19	3/23	3/25	3/27	3/30	1	1
Avg.	**7**		**1,187,813**						**2.00**	**1.57**
		Sum	8,314,688							
GRA8500	aa846222	USD	247,426	3/1	3/1	3/3	3/7	3/8	2	3
	aa789322	USD	1,234,486	3/1	3/2	3/5	3/6	3/10	3	0
	aa156855	USD	2,154,438	3/13	3/14	3/18	3/21	3/22	3	2
	aa264355	USD	755,923	3/17	3/17	3/18	3/25	3/26	0	8
	bb789211	USA	511,023	3/5	3/5	3/5	3/7	3/11	1	1
	bb415663	USA	986,321	3/8	3/9	3/14	3/16	3/17	4	2
	bb231555	USA	1,423,899	3/11	3/12	3/14	3/15	3/16	1	0
	cc782466	Canada	1,123,894	2/28	3/1	3/3	3/4	3/4	2	0
	cc123255	Canada	953,014	3/4	3/5	3/9	3/12	3/13	3	2
	cc446533	Canada	2,562,216	3/7	3/8	3/10	3/12	3/14	2	2
	cc879511	Canada	2,265,843	3/10	3/10	3/13	3/14	3/14	2	2
	cc192522	Canada	982,168	3/10	3/11	3/18	3/21	3/22	6	1
	cc7521	Canada	326,521	3/10	3/12	3/13	3/15	3/17	1	3

	3									
	cc18743	Canada	1,853,254	3/18	3/18	3/22	3/26	3/27	3	1
	dd32119	Europe	1,325,648	3/12	3/13	3/14	3/19	3/21	1	0
	dd48916	Europe	632,589	3/16	3/17	3/18	3/21	3/22	0	2
	dd15234	Europe	1,100,032	3/16	3/16	3/19	3/27	3/27	2	6
	dd14625	Europe	2,014,895	3/20	3/21	3/26	3/28	3/30	4	0
	ee32456	Japan	1,532,649	3/1	3/1	3/3	3/6	3/10	2	2
	ee78921	Japan	785,321	3/2	3/3	3/5	3/7	3/10	1	1
Avg.	**20**		**1,238,578**						**2.15**	**1.90**
		Sum	24,771,560							
GZN0100	aa54889	USD	854,622	2/28	2/28	3/4	3/7	3/7	3	2
	aa25466	USD	118,562	3/5	3/6	3/12	3/14	3/15	3	1
	aa52166	USD	1,986,523	3/17	3/17	3/20	3/25	3/25	4	4
	aa26799	USD	985,246	3/18	3/18	3/21	3/22	3/25	0	0
	aa98755	USD	1,152,356	3/21	3/23	3/24	3/29	3/30	4	4
	bb79882	USA	1,895,324	3/1	3/4	3/9	3/15	3/16	8	5
	bb3554	USA	77,595	3/13	3/14	3/17	3/22	3/23	3	4

	6									
Avg.	**7**		**1,010,033**						**3.57**	**2.86**
		Sum	7,070,228							
GZN2000	bb78532	USA	1,123,489	2/22	2/23	2/26	2/28	3/1	2	2
	bb16244	USA	2,010,689	3/11	3/15	3/20	3/26	3/31	4	4
	bb98523	USA	650,244	3/14	3/15	3/18	3/24	3/25	3	5
	bb78516	USA	2,341,568	3/16	3/18	3/25	3/28	3/29	8	2
	ee12446	Japan	1,256,384	3/2	3/4	3/6	3/8	3/10	1	1
	ee87952	Japan	986,523	3/12	3/12	3/15	3/18	3/19	1	2
	T16211	Test	785,622	2/27	3/1	3/3	3/10	3/16	2	5
	T78992	Test	1,235,891	3/15	3/16	3/22	3/27	3/27	7	4
Avg.	**8**		**1,298,801**						**3.50**	**3.13**
		Sum	10,390,410							
XTL0001	aa21622	USD	2,423,168	3/1	3/2	3/4	3/9	3/11	2	4
	aa38545	USD	1,982,548	3/6	3/7	3/11	3/16	3/16	3	5
	aa79532	USD	1,652,384	3/7	3/7	3/8	3/14	3/15	0	5
	aa72465	USD	2,452,162	3/10	3/12	3/16	3/21	3/21	4	3
	aa89456	USD	1,152,689	3/15	3/15	3/18	3/24	3/24	2	7

	ee48922	Asia	1,895,231	2/26	2/26	3/3	3/4	3/4	6	0
	ee00162	Asia	2,006,159	3/12	3/12	3/15	3/20	3/21	2	4
	T01508	Test	1,895,211	3/2	3/3	3/10	3/14	3/5	5	6
	T07892	Test	2,789,352	3/18	3/20	3/21	3/25	3/26	2	3
Avg.	**9**		**2,027,656**						**2.89**	**4.11**
		Sum	18,248,904							

Table 4: Month 4 Traveler Data

Technology	Device ID#	Country	# of Transistors	Receive Date	Data Check	Physical Test	Logical Test	Mask Format	Incidents of Physical Failure	Incidents of Logical Failure
GRA7000	aa48246	USD	1,523,284	4/1	4/1	4/4	4/6	4/7	3	1
	bb15665	USA	859,624	4/7	4/8	4/13	4/17	4/17	3	2
	cc78952	Canada	1,245,384	4/6	4/6	4/8	4/11	4/13	1	3
	cc23458	Canada	1,002,345	4/20	4/22	4/25	4/30	4/30	2	5
	ff78921	Asia	750,816	4/12	4/12	4/13	4/15	4/16	0	1
Avg.	**5**		**1,076,291**						**1.80**	**2.40**

		Sum	5,381,453							
GRA8500	aa48922	USD	542,326	3/29	3/30	4/2	4/6	4/6	2	3
	aa12358	USD	1,852,645	4/3	4/4	4/7	4/11	4/13	2	3
	aa78944	USD	1,752,462	4/7	4/8	4/13	4/16	4/16	4	2
	aa32556	USD	1,125,324	4/14	4/15	4/17	4/20	4/20	1	1
	cc12456	Canada	652,301	4/6	4/6	4/9	4/11	4/12	2	2
	cc78251	Canada	1,452,632	4/20	4/21	4/25	4/27	4/27	3	1
	dd32455	Europe	502,138	3/30	4/1	4/4	4/6	4/6	2	2
	dd21685	Europe	1,185,642	4/2	4/4	4/7	4/11	4/13	3	3
	dd24562	Europe	1,562,789	4/16	4/16	4/19	4/20	4/23	2	0
	dd98251	Europe	982,465	4/17	4/18	4/22	4/25	4/26	4	2
	ee21564	Japan	1,100,562	4/5	4/5	4/6	4/8	4/9	2	1
	ee53268	Japan	2,018,984	4/8	4/9	4/11	4/13	4/13	1	1
Avg.	**12**		**1,227,523**						**2.33**	**1.75**
		Sum	14,730,270							
GZN0100	aa25489	USD	985,215	3/25	3/26	3/30	4/2	4/4	6	2

	aa12654	USD	1,526,488	3/30	3/30	4/4	4/7	4/8	3	1
	aa89543	USD	1,852,624	4/6	4/7	4/10	4/12	4/13	2	1
	aa21685	USD	765,216	4/7	4/9	4/13	4/16	4/17	3	2
	aa01249	USD	3,205,615	4/12	4/13	4/15	4/17	4/17	0	2
	aa88624	USD	854,216	4/15	4/17	4/22	4/25	4/26	3	1
	aa42689	USD	1,523,849	4/18	4/19	4/22	4/26	4/27	1	5
	aa12452	USD	1,268,489	4/18	4/19	4/24	4/27	4/29	4	2
	aa78216	USD	1,652,489	4/22	4/23	4/26	4/30	4/30	2	4
	bb21234	USA	650,254	4/1	4/1	4/5	4/10	4/11	3	4
	bb12621	USA	854,261	4/5	4/5	4/7	4/8	4/9	3	0
	bb75982	USA	1,253,498	4/6	4/7	4/9	4/16	4/16	1	8
	bb12485	USA	1,685,124	4/10	4/10	4/14	4/17	4/18	4	2
	bb98215	USA	895,216	4/12	4/12	4/17	4/21	4/21	6	3
	bb65328	USA	1,895,324	4/14	4/15	4/19	4/23	4/24	3	4
	bb84465	USA	1,102,658	4/18	4/18	4/22	4/28	4/30	5	5
Avg.	**16**		**1,373,159**						**3.06**	**2.88**

		Sum	21,970,536							
GZN2000	aa24589	USD	851,565	4/1	4/2	4/6	4/11	4/12	3	4
	aa12652	USD	1,258,267	4/15	4/15	4/18	4/22	4/22	2	3
	bb78215	USA	1,856,982	3/29	4/1	4/6	4/9	4/10	5	2
	bb24156	USA	1,526,489	4/8	4/9	4/13	4/17	4/18	3	5
	bb89251	USA	785,216	4/10	4/11	4/16	4/18	4/21	6	2
	bb25051	USA	1,985,246	4/18	4/20	4/23	4/28	4/30	1	3
	cc89245	Canada	854,261	4/6	4/7	4/18	4/26	4/27	6	6
	ee21558	Japan	2,152,008	4/1	4/2	4/5	4/17	4/18	2	3
	ee89153	Japan	856,248	4/2	4/2	4/6	4/11	4/12	3	4
	T26245	Test	500,897	4/10	4/11	4/14	4/19	4/20	2	2
	T46259	Test	3,652,165	4/16	4/17	4/21	4/26	4/27	4	6
Avg.	**11**		**1,574,390**						**3.36**	**3.64**
		Sum	14,169,512							
XTL0001	aa74165	USD	1,892,165	3/25	3/25	3/28	3/30	4/1	2	0
	aa85426	USD	1,524,328	3/30	3/30	4/3	4/8	4/9	4	3
	aa13254	USD	859,246	4/6	4/8	4/13	4/16	4/16	5	4

	aa98562	USD	2,152,084	4/10	4/11	4/15	4/20	4/21	3	4
	aa12453	USD	1,652,385	4/11	4/11	4/15	4/18	4/22	4	2
	bb25168	USA	1,952,462	4/8	4/10	4/12	4/16	4/17	1	3
	bb15248	USA	1,253,658	4/17	4/18	4/19	4/23	4/23	2	2
	dd84526	Europe	1,854,268	4/2	4/4	4/7	4/12	4/13	2	4
	dd01528	Europe	985,123	4/5	4/6	4/10	4/15	4/16	3	5
	dd32588	Europe	650,848	4/11	4/11	4/13	4/21	4/21	1	7
	ee21685	Japan	1,652,498	4/13	4/14	4/16	4/18	4/20	0	1
	ff15895	Asia	1,985,216	4/3	4/5	4/8	4/10	4/13	2	2
	T12024	Test	1,526,312	4/8	4/9	4/10	4/16	4/16	1	5
	T24985	Test	842,168	4/16	4/17	4/22	4/25	4/25	6	2
Avg.	**14**		**1,484,483**						**2.57**	**3.14**
		Sum	20,782,761							
XTL1001	T12585	Test	852,325	4/5	4/5	4/11	4/19	4/21	5	7
	T48985	Test	1,759,532	4/9	4/11	4/14	4/20	4/21	2	5
Avg.	**2**		**1,305,929**						**3.50**	**6.00**
		Sum	2,611,857							

Exhbit 3: Time Study (hours)

Process	Manual	Std. Dev	Computer	
Receive Data	2.550	0.550	2.067	0.250
Physical Test	0.400	0.217	1.500	1.750
Logical Test	0.217	0.100	3.150	2.133
Mask Format	0.550	0.067	0.767	0.267

* Actual Average and Standard Deviation for 1 pass of 1 design
** Does not include monitoring times

Exhibit 4: Demand

Overall Forecast

	Month				
Technology	9	10	11	12	Totals
GRA6000	2	0	0	0	2
GRA7000	3	3	0	0	6
GRA8500	6	10	16	8	40
GZN0100	21	16	9	8	54
GZN2000	14	10	12	9	45
XTL0001	10	15	18	25	68
XTL1001	2	7	10	16	35
Totals	58	61	65	66	250

Breakdown by Technology

GRA6000	Month			
	9	10	11	12
USD	2	0	0	0
USA	0	0	0	0
Canada	0	0	0	0
Europe	0	0	0	0
Japan	0	0	0	0
Asia	0	0	0	0
Test	0	0	0	0

GRA7000	Month			
	9	10	11	12
USD	1	0	0	0
USA	0	0	0	0
Canada	2	3	0	0
Europe	0	0	0	0
Japan	0	0	0	0
Asia	0	0	0	0
Test	0	0	0	0

GRA8500	Month			
	9	10	11	12
USD	1	2	5	3
USA	0	0	0	0
Canada	0	4	6	3
Europe	3	2	3	2
Japan	2	2	2	0
Asia	0	0	0	0
Test	0	0	0	0

GZN0100	Month			
	9	10	11	12
USD	11	9	3	2
USA	10	7	6	4
Canada	0	0	0	0
Europe	0	0	0	0
Japan	0	0	0	0
Asia	0	0	0	0
Test	0	0	0	2

GZN2000	Month			
	9	10	11	12
USD	2	3	2	3
USA	5	3	4	4
Canada	0	0	0	0
Europe	0	0	0	0
Japan	4	3	4	0
Asia	0	0	2	0
Test	3	1	0	2

XTL0001	Month			
	9	10	11	12
USD	3	4	6	5
USA	2	1	2	3
Canada	0	0	2	4
Europe	4	4	3	2
Japan	0	0	2	5
Asia	1	2	2	3
Test	0	2	1	3

XTL1001	Month			
	9	10	11	12
USD	0	3	2	4
USA	0	2	4	5
Canada	0	0	0	0
Europe	0	0	1	2
Japan	0	0	0	0
Asia	0	1	3	3
Test	2	1	0	2